Amendments to the Specification:

Please replace paragraph [0008] with the following amended paragraph:

[0008] However, related art implementation such as that shown in Figure 3 have several problems. First, in such a design there are only two possible signal path lengths. Thus, such a system would not compensate for the situation where the optimum signal path length is somewhere between the short path 16 and the long path 18 lengths. In such a situation, system designers typically choose the shorter path length and ~~compensated~~ compensate by adding capacitance. Adding capacitance, while having the effect of slowing the rise times associated with that clock, may only be used to a certain extent before clock signal degradation becomes a problem.

Please replace paragraph [0024] with the following amended paragraph:

[0024] Referring now to Figure 4, computer system 200, in accordance with the preferred embodiment preferably comprises a micro-processor or CPU 50 coupled to a main memory array 52 through an integrated bridge logic device 54. As depicted in Figure 4, the bridge logic device 54 is sometimes referred to as a "North bridge," based generally upon its location within a computer system drawing. The CPU 50 preferably couples to the bridge logic 54 via a CPU bus 56, or the bridge logic 54 may be integrated into the CPU 50. The CPU 50 preferably comprises a ~~Pentium~~ Pentium III® microprocessor manufactured by Intel®. It should be understood, however, that other alternative types and brands of microprocessors could be employed. Further, an embodiment of computer system 100 may include multiple processors, with each processor coupled through the CPU bus 56 to the bridge logic unit 54. To increase memory capability, and memory bus bandwidth, multiple bridge logic units 54 may be used, each coupled to its own main memory array 52.

Please replace paragraph [0032] with the following amended paragraph:

[0032] Assuming for purposes of explanation that a system designer wishes to implement path 88 between pads 82 and 84, during the process of installing the various components on the motherboard or other PCB card, only resistors 94A and 94B are installed. Thus, the PLL clock signal propagates from the control signal source PLL 78 to the pad 82 (across ~~the unnumbered resister~~ resistor 102 which is described in more detail below), up through resistor 94A across the signal path 88, down through resistor 94B and to the second pad 84. In this exemplary embodiment, none of the resistors 94C-94F would be installed and thus no electrical path would exist along signal paths 90 and 92. Moreover, the system designer also preferably makes adjustments to the overall control signal path by selectively installing resistors 94G-94L in the second cluster of signal paths shown in Figure 5. For example, the system designer may implement the signal path 96 of the second cluster so that the overall signal path comprises the trace length from the PLL to the first pad, from the first pad along path 88 to the second pad, from the second pad 84 along path 96 to the third pad 86, and from the third pad 86 to the control signal destination, which in Figure 5 is the memory controller 58.

Please replace paragraph [0033] with the following amended paragraph:

[0033] It is assumed, but not required, that each of the traces 88, 90 and 92 in the first cluster, and traces 96, 98 and 100 in the second cluster, have a different length. Thus, a system designer may choose a plurality of different signal path lengths by selectively installing resistors 94A-94L. Still referring to Figure 5, and assuming that the signal path lengths are substantially as shown in Figure 5, it is seen that the shortest path for the clock signal to travel from the PLL 78 to the memory controller 58 is through the first cluster by way of signal path 90, and through the second cluster by way of signal path 98. Likewise, in the exemplary embodiment of Figure 5, the longest path length could be implemented by the clock signal traveling through the first cluster by way of signal path 88 or 92 and through the second cluster by way of signal path 96 or 100.

Please replace paragraph [0034] with the following amended paragraph:

[0034] Although embodiments that have duplicate signal path lengths among the various clusters are within the contemplation of this invention, in the preferred embodiment each of the signal path lengths are different, thereby allowing the system designer the maximum number of possible signal path lengths with which to tune the timing signals in the computer system 200. Referring now to Figure 6 there is shown an embodiment similar to that of Figure 5 for purposes of explaining the benefits and advantages of having signal paths with varying lengths. In particular, Figure 6 shows the signal paths of the first cluster, comprising paths A, B, and C, and the signal paths of the second cluster D, E, and F. Further assume that each of these signal paths A-F have a length (of arbitrary unit) as indicated in Table 1.

A	0.25
B	0.5
C	0.75
D	1.0
E	1.25
F	1.50

TABLE 1

Table 1 shows that for this embodiment, each of the signal paths A-F have a length different than the others ranging from 0.25 units to 1.50 units. The units of these lengths could be any length included but not limited to inches and centimeters. The unit of length desired is a function of the amount of delay required in the particular system. An adjustable signal path circuit 80 having the signal path lengths described in Table 1 gives a total of 9 unique signal paths through the signal path circuit. In particular, Table 2 shows each unique signal

path, and that signal path's length given the arbitrary units assigned in Table 1.

AD	1.25
AE	1.5
AF	1.75
BD	1.5
BE	1.75
BF	2.0
CD	1.75
CE	2.0
CF	2.25

TABLE 2

Table 2 thus shows that for the unique path through the adjustable signal path circuit 80 comprising the signal paths A and D of Figure 6 (AD in Table 2), the total length given the assigned values in Table 1 is 1.25 units. Similarly, unique path AE has a length of 1.5 units. Thus, Table 2 shows that for the two cluster system, each cluster containing three possible paths, there are nine unique signal paths that the clock signal may take. Table 2 also exemplifies that even using the path lengths given in Table 1, where each path length is different, there are still duplicate overall path lengths. In particular, Table 2 shows that path AE is equivalent in length to path BD, path AF is equivalent in length to BE and CD, and path BF is equivalent in length to path CE. Although an embodiment of the present invention could use an adjustable signal path circuit where some of the multiple unique paths have the same length, preferably the lengths of the signal paths are selected such that no two signal paths through the adjustable signal path circuit have the same length. While there may be many possible selections for signal paths that do not give duplicate lengths, Table 3 shows an exemplary selection for the path lengths that gives an overall adjustable signal path circuit selection ranging from 1.33 units to 4.0 units.

A	1
B	2
C	3
D	.33
E	.66
F	1.0

TABLE 3

AD	1.33
AE	1.66
AF	2.0
BD	2.33
BE	2.66
BF	3.0
CD	3.33
CE	3.66
CF	4.0

TABLE 4

Thus, it is seen that the unit lengths assigned in Table 3 (which could realistically be of the units inches) gives signal path lengths of Table 4 ranging from 1.33 units to 4.0 units, with each increment mapping to approximately 1/3 of a unit length.

Please replace paragraph [0039] with the following amended paragraph:

[0039] Thus, it is seen that the embodiments of the invention give the system designer a topology for signal timing adjustments that is highly flexible and may be easily and precisely tuned for the particular components on the motherboard or PCB card. Referring back to the computer system 200 shown in Figure 4, an adjustable signal path circuit 80 could be implemented anywhere in the computer system where the system designer needs to vary the length of a signal path, be it for a clock circuit or any other control signal propagating within the computer system. Preferably, however, the timing constraints between the memory controller ~~58~~ 57 and the main memory array 52 may require that the clock signals feeding each of these devices (it is noted that the memory controller 58 has a clock signal both from the host clock 76 and the PLL 78) preferably implement one of these variable length signal path circuits so that the timing signals for reads and writes between them may be adjusted.